REMARKS

The office action mailed March 1, 2002, has been carefully reviewed and these remarks are responsive thereto.

In an Information Disclosure Statement filed on Dec. 6, 2001, Applicants indicated that this application relies, under 35 U.S.C. § 120, on the earliest filing date of prior U.S. patent application serial no. 09/505,204, filed February 16, 2000, which has issued as U.S. Patent No. 6,359,480 since the filing of this application. The Information Disclosure Statement further indicated that the documents identified on the attached PTO 1449 form were submitted to and/or cited by the Office in a prior application and, therefore, copies are not required to be provided in this application. Nevertheless, the PTO 1449 indicates that while the U.S. patent documents were considered, the foreign patent documents were not, with a notation that the references were deemed "not available." Although the Applicants' initial submission was in compliance with the requirements of 37 C.F.R. § 1.98(d) for consideration of the references cited in the original PTO 1449, Applicants have attached a revised PTO 1449 including citations to only those foreign patent references that have not been considered, along with copies of those documents, to facilitate their consideration. Because Applicants' original submission was in compliance with 37 C.F.R. § 1.98(d), no additional fees are due in accordance with Applicants submission of the revised PTO 1449.

The Office Action rejects originally filed claims 1-6. Specifically, the Office Action rejects claims 1-2 and 6 as being anticipated under 35 U.S.C. § 102 by Park et al. (U.S. Patent No. 5,682,113). Claims 1, 3 and 6 stand rejected as being anticipated under 35 U.S.C. § 102 by

Isobe et al. (U.S. Patent No. 4,933,579). Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Park et al. in view of D'Souza et al. (U.S. Patent No. 5,606,270). The rejection of the claims over the prior art of record has been rendered moot by the amendment to independent claims 1 and 6, as has the rejection of the claims depending therefrom (claims 2-5).

The Office Action, at page 2, asserts that Park et al. discloses, as illustrated in Figure 4, an apparatus comprising, "a delay circuit 210 for receiving a first pulse (output of 131); and a logic circuit (NOR gate 220) coupled to the output of the delay circuit and an inverted signal of the first pulse (via inverter 132)." The claims as amended, however, recite "a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and a logic circuit to which a second pulse signal output from said clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction." Inverter 132 disclosed in Park et al. does not correspond to the claimed clocked inverter circuit changing a pulse width of the first pulse in a first direction and NOR gate 220 disclosed in Park et al. does not output a third pulse signal whose pulse width is changed to a second direction opposite to the first direction, as claimed. Thus, at a minimum, Park et al. fails disclose each and every feature of independent claims 1 and 6.

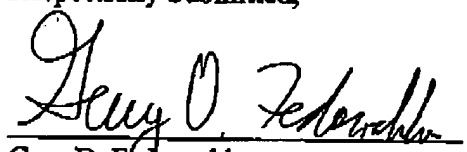
The Office Action, at page 2, asserts that Isobe et al. discloses, as illustrated in Figure 4, an apparatus comprising "a delay circuit 12 for receiving a first pulse Si, and a logic circuit (NAND gate 14) coupled to the output of the delay circuit and an inverted signal of the first pulse (via inverter 13)." The claims as amended, however, recite, "a clocked inverter circuit to

which a first pulse signal is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and a logic circuit to which a second pulse signal output from said clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction." Inverter 13 disclosed in Isobe et al. does not correspond to the claimed clocked inverter circuit changing a pulse width of the first pulse in a first direction and NAND gate 14 disclosed in Park et al. does not output a third pulse signal whose pulse width is changed to a second direction opposite to the first direction, as claimed. Accordingly, Isobe et al. fails to teach each and every feature claimed in independent claims 1 and 6.

New claims 7-15 are fully supported in the specification and are considered allowable over the art of record. For example, independent claim 11 includes unit delay elements which are absent from the art of record.

Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same. If any questions remain, the Examiner is invited to contact the undersigned to further prosecution.

Respectfully Submitted,

By: 

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Dated: June 25, 2002

MARKED UP VERSION OF AMENDMENT

IN THE SPECIFICATION

Please amend the application as follows:

[01] This application is a divisional of U.S. patent application serial no. 09/505,204, filed February 16, 2000, which issued on March 19, 2002 as U.S. Patent No. 6,359,480, which is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-038574, filed February 17, 1999, the entire contents of which are incorporated herein by reference.

IN THE CLAIMS

Please amend claims 1 and 6 as follows.

1. (Amended) A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal outputted from said clocked inverter circuit and ~~the~~an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction ~~wherein~~

~~said clocked inverter circuit changes the pulse width of said first pulse signal in the direction opposite to the direction in which a pulse width of a third pulse signal outputted from said logic circuit changes.~~

4. (Amended) The delay circuit according to claim 1, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor and at least one of a channel width, channel length, threshold voltage, and substrate voltage of the NMOS transistor is different from a channel width, channel length, threshold voltage, and substrate voltage of the PMOS transistors.

5. (Amended) The delay circuit according to claim 4, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set to a value other than one and a rise time of ~~a~~said first pulse signal is made different from a decay time of ~~the~~said first pulse signal.

6. (Amended) A delay circuit comprising:

an inverter circuit controlled by a clock signal to which ~~an~~ first pulse signal is supplied, said inverter circuit changing a pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal outputted from said inverter circuit and ~~the~~an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction[~~wherein~~

~~said clocked inverter circuit changes the pulse width of said input pulse signal in the direction opposite to the direction in which the pulse width of the pulse signal outputted from said logic circuit changes~~].

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete If Known	
Application Number	TBA
Filing Date	Herewith
First Named Inventor	Katsuaki ISOBE et al.
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	001701.00129

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3,920,962	B1	Mayer et al.	11-18-1975	
		4,237,422	B1	Lenhardt	12-02-1980	
		4,710,648	B1	Hanamura et al.	12-01-1987	
		5,287,025	B1	Nishimichi	02-15-1994	
		5,438,550	B1	Kim	08-01-1995	
		5,498,989	B1	Diba	03-12-1996	
		5,671,214	B1	Tanaka	09-23-1997	
		5,867,432	B1	Toda	02-02-1999	
		6,069,508	B1	Takai	05-30-2000	
		6,140,855	B1	Kirihata et al.	10-31-2000	
		6,141,127	B1	Boivin et al.	10-31-2000	

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP	10-069326	A	Toshiba	03-10-1998		Abst
		JP	11-316706	A	Toshiba	11-16-1999		Abst

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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